Neural Stimulating CMOS Chip
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Motivation

Develop a fully implantable bioelectronics system, capable of interfacing with neural systems in a bidirectional manner (recording and stimulation), specifically for log-term, free-roaming, small animal neuroscience research. The implantable system includes a multi-electrode neural stimulating and recording CMOS integrated circuit with wireless power and data telemetry capability (Prof. Hashemi’s group), parylene microelectrode arrays (Prof. Meng’s group), and other necessary components in a proper package (Prof. Weiland’s group). The envisioned experiments using this platform by neuroscientist collaborators (Prof. McGee’s and Prof. Berger’s groups) include experiments in visual cortex plasticity, experiments in visual mid-brain plasticity, and hippocampal studies to identify neural behaviors of untouched animals in complex environments.

State of the Art

• Single- and multi-electrode neural stimulating integrated circuits, realized in CMOS, have been reported by research groups and are offered by companies (e.g., Intan Technologies).
• Shortcomings of the existing solutions
  • Power inefficient

Innovative Approaches & Design Features

• Adjust the level of DC power supply of the current stimulator as a function of stimulating current to ensure a low dropout voltage across stimulating devices and maintain high efficiency across a wide range of stimulating current and load values.
• Switched-capacitor DC-DC voltage converters with shared capacitors generate the necessary DC power supplies.
• Charge-balancer ensures zero net-charge accumulation/depletion in the tissue (load).

Two stimulating modes:
1. Pre-programmed biphasic waveform with controllable pulse intervals (5 bits for each instance)
   • t_s, t_tr, and t_i and amplitude (4 bits for each amplitude A_h, A_m, A_l, and A_n).
2. Arbitrary waveform — every 50 µs a new latched pulse may be sent to the chip from an external source.

• Amplitude of the stimulating current may vary within -100 µA to +100 µA in 100 µA steps.
• The load can vary from a few kΩ to 40 kΩ to accommodate for different electrode sizes and implant locations.

Neural Stimulator Chip Architecture

Current Source Blocks

DC-DC Converter

Circuit Building Blocks

Charge Balancer

During the waiting time between consecutive cycles (user controlled), short current pulses cancel any memorized charge on the electrode. This voltage drop across the safety resistor.

Chip Layout (130nm CMOS)

Simulated Results

Future Work

• Other methods to increase current source efficiency will be investigated.
• Neural signal recording system will be designed addressing 2 main challenges:
  1) Area per channel (<40 µm x 40 µm)
  2) Power per channel (< 1 µW)
• Stimulating and recording systems will be integrated on a single chip, with wireless power and data telemetry capability.

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